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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,688	12/27/2001	Kazushi Fujimoto	Q67203	9334

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EXAMINER	
SHANKAR, VIJAY	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,688	FUJIMOTO ET AL.	
	Examiner	Art Unit	
	VIJAY SHANKAR	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *24-38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *17-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (Claims 1-23) in the reply filed on 12-30-2005 is acknowledged. Non-Elected Claims 24-38 should be cancelled.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuboki et al (5,790,165).

Regarding Claim 1, Kuboki et al teaches a method of driving a liquid crystal display device having a plurality of bus lines for transmitting image data, the method comprising: branching original image data having an original data rate into branched plural-systems image data comprising plural systems having a converted data rate which is equal to either the original data rate or a half of the original data rate (Summary; Figs.15-17; Col.15, line 50- Col. 18, line 50);

supplying a source driver circuit with the branched plural-systems image data in synchronizing with at least a clock signal having a clock frequency (Figs.15,17; Col.15, line 50- Col. 18, line 50) which is a quarter of the original data rate (Fig.32-34; Col.24, line 44 - Col. 25, line 7); and allowing the source driver to further branch the branched plural-systems image data into gray scale voltage signals. (Figs.6-7; Col.10, line 42- Col.11, line 35; Figs.15,17; Col.15, line 50- Col. 18, line 50).

Regarding Claims 2-3 and 10-11, Kuboki et al teaches a method wherein the number of the systems of the branched plural-systems image, data is 2J, where J is a positive integer number, and the number of the systems of the branched plural-systems image data is 4J, where J is a positive integer number. (Figs.18-20; Col.18, line 54- Col.19, line 10).

Regarding Claims 4 and 12, Kuboki et al teaches a method wherein the converted data rate is equal to the original data rate. (Figs.15-17; Col.15, line 50- Col. 18, line 50).

Regarding Claims 5 and 13, Kuboki et al teaches a method wherein the converted data rate is equal to a half of the original data rate. (Figs.15-17).

Regarding Claims 6 and 14, Kuboki et al teaches a method wherein the at least a clock signal comprises two clock signals different in phase by a half cycle from each other, and rising edges of the two clock signals serve as triggers to input the image data into the source driver. (Figs.15-17; Col.15, line 50- Col. 18, line 50).

Regarding Claims 7 and 15, Kuboki et al teaches a method wherein the at least a clock signal comprises two clock signals different in phase by a half cycle from each other, and falling edges of the two clock signals serve as triggers to input the image data into the source driver. (Figs.15-17; Col.15, line 50- Col. 18, line 50).

Regarding Claims 8 and 16, Kuboki et al teaches a method wherein the at least a clock signal comprises a single clock signal, and both rising edges and falling edges of the single clock signal serve as triggers to input the image data into the source driver. (Figs.15-17; Col.15, line 50- Col. 18, line 50).

Regarding Claim 9, Kuboki et al teaches a circuitry for driving a liquid crystal display device (Fig.15), the circuit comprising: a timing controller (3121 in fig.15) for generating image data and at least a clock signal (Col.16, lines 34-67); a plurality of data bus lines (205 in fig.7) for transmitting the image data and at least a clock signal (Fig.7; Col.11, line 7-32) ; and a plurality of source driver circuits for incorporating the image data in synchronizing with the at least a clock signal and converting the image

data into gray scale voltage signals (Figs.15-17; Col.15, line 50- Col. 18, line 50), wherein the timing controller includes: a branching unit for branching original image data having an original data rate into branched plural-systems image data comprising plural systems having a converted data rate which is equal to either the original data rate or a half of the original data rate (Figs.15,17; Col.15, line 50- Col. 18, line 50).

5. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

6. Claims 17-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an examiner's statement of reasons for allowance: The prior arts Kuboki et al (5,790,165) fails to teach a circuitry for driving a liquid crystal display device wherein the timing controller further includes: a data polarity inversion determination unit for verifying whether or not a majority of bits of the branched plural-systems image data is changed in polarity; and a data polarity inversion unit for inverting all bits of the branched plural-systems image data in polarity if it is verified that

the majority of bits of the branched plural-systems image data is changed in polarity as claimed in Claim 17.

The prior arts Kuboki et al (5,790,165) fails to teach a circuitry for driving a liquid crystal display device wherein the timing controller further includes: a first latch circuit for latching the branched plural-systems image data in synchronizing with the at least a clock signal and outputting the branched plural-systems image data as first output data; a first data polarity inversion determination circuit for inverting all bits of the branched plural-systems image data in polarity if a first polarity inversion signal has a predetermined level which indicates polarity inversion, and the first data polarity inversion determination circuit also outputting polarity-inverted image data; a second data polarity inversion determination circuit for comparing the polarity-inverted image data and the branched plural-systems image data to verify whether or not a majority of bits of the polarity-inverted image data is different in polarity from the branched plural-systems image data, and the second data polarity inversion determination circuit also outputting a second polarity inversion signal which has a predetermined level which indicates polarity inversion, if the majority of bits of the polarity-inverted image data is different in polarity from the branched plural-systems image data; and a second latch circuit for latching the second polarity inversion signal in synchronizing with the at least a clock signal and supplying the first polarity inversion signal to the first data polarity inversion determination circuit as claimed in Claim 20.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIJAY SHANKAR whose telephone number is (571) 272-7682. The examiner can normally be reached on M-F 7:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIJAY SHANKAR
Primary Examiner
Art Unit 2673

VS